

ELEG 3923
MICROCONTROLLER SYSTEM DESIGN
Spring, 2007

INSTRUCTOR

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COURSE DESCRIPTION

Introduction to 16-bit microcontrollers and their application. Microcontroller architecture, addressing modes and instruction set. Assembler and emulator experience. Programming techniques and applications. Computer timing , bus usage and system memory design. Input/Output including parallel, serial and A/D conversion. Laboratory exercises to demonstrate, and enhance the understanding and implementation of, microcontroller system design.

COURSE TEXTS

68HC12 Microcontroller Theory and Applications, D. Pack and S. Barrett,
Prentice Hall, 2002 (ISBN 0-13-033776-5)
(with CD-ROM containing cross-assembler and simulator programs)

COURSE PREREQUISITES

Digital logic Operations (combinational and sequential) and gates
Math operations in, and conversion between, Binary, Decimal, Hex and BCD
Computer Math - signed numbers and 2's complement
Ability to write and understand programs in the C language

COURSE GOALS

At the conclusion of this course, the student should be able to:

1. Understand and describe the microcontroller's internal and external structure as well as the typical instruction cycle and program execution.
2. Interface a microcontroller with its external environment
3. Program the 68HC12 in assembly language to perform a task
4. Design a Microcontroller System including external memory

COURSE GRADING

Three one-hour exams @ 100 points each:	300
In-class Learning Evaluations	100
Final Exam:	150
Laboratory Points	100
Total Points Possible:	650

Scores in the following ranges will guarantee the grades indicated:

<u>Total Points</u>	<u>Grade</u>
585 - 650	A
520 - 584	B
455 - 519	C
390 - 454	D
< 390	F

I reserve the right to adjust any or all ranges downward (e.g. 500 - 584 may be the "B" range) if course performance indicates it is appropriate.

RULES OF THE GAME

The pace of the course will be rapid and it is imperative that you keep up with the class! To help you in this, there will be homework assigned almost every class period and you are strongly encouraged to attempt to complete this before the next class. Class attendance is not compulsory but highly recommended.

Exam #1 February 15

Exam #2 March 29

Exam #3 May 1

The **final exam** will be **Tuesday, May 8 from 12:30 to 2:30**

Make-up exams will not be given except by pre-arrangement or last minute emergencies.

A lab is an integral part of this course. Labs will meet as indicated on the attached Lecture/Lab schedule.

I hope you find this course enjoyable, interesting and intellectually challenging. My door is almost always open if I am in the office. Please feel free to stop by. You can also schedule an appointment via phone or e-mail.

INCLEMENT WEATHER POLICY

If the University remains open, it is my intent to conduct class. However, if the university remains open but there is serious snow and ice to the point where I cannot reach the university, I will, if at all possible, put a message on my answering machine at home (521-2148) indicating that class is canceled two hours before the scheduled class time . If the University is open and if class will be conducted as scheduled, there will not be any weather-related message on my answering machine. Do not take any serious risk in reaching class if you feel the weather is too bad for you to travel.

ELEG 3923 Course Lecture Schedule for Spring, 2007

Date	Lecture #	Topics
1/16	1	Introduction, Elements of a basic computer
1/18	2	Elements of a Basic Computer, Software, Overview of HC12
1/23	3	HC12 Instruction Set
1/25	4	Programming, Assembler Directives
1/30	5	<i>Lab #1 Text Lab Chapter Two A and B</i>
2/1	6	The Assembly Process, Hand Assembly, Stack
2/6	7	Subroutines, Flowcharting
2/8	8	<i>Lab #2 Text Lab Chapter Three A and B</i>
2/13	9	Review for Test #1
2/15	10	Test #1
2/20	11	HC12 Hardware, Port System Timer Module, Memory, Interrupts, Switches,
2/22	12	Keypads
2/27	13	Resets
3/1	14	<i>Lab # 3 Text Labs Chapter Five and Chapter Six</i>
3/6	15	Interrupts, clock module
3/8	16	Timer, free-running counter, input capture,
3/13	17	output compare, Pulse Accumulator
3/15	18	<i>Lab #4 Text Lab Chapter Seven A</i>
3/27	19	<i>Lab #4 Continued Text Lab Chapter Seven B</i>
3/29	20	Test #2
4/3	21	Introduction to A2D and DAC
4/5	22	HC12 ATD
4/10	23	ATD Control Registers
4/12	24	<i>Lab # 5 New A2D Lab - to be developed</i>
4/17	25	ATD Programming Application and Register Block Mapping
4/19	26	Memory System Design I
4/24	27	Memory System Design II
4/26	28	<i>Lab # 6 New Memory Design Lab - to be developed</i>
5/1	29	Test # 3
5/3	30	Course Review
5/8	Tuesday	Final Exam 12:30 PM