ELEG 4233 – INTRODUCTION TO INTEGRATED CIRCUIT DESIGN

Credits and Contact Hours

Three credit hours, 45 hours of instructor contact

Instructor's Name

Randy Brown

Textbook

CMOS VLSI Design: A Circuits and Systems Perspective, Neil Weste and David Harris, 2011

Specific Course Information

a. Catalog Description
   ELEG 4233. Introduction to Integrated Circuit Design. Credit 3. Design and layout of large scale digital integrated circuits using CMOS technology. Topics include MOS devices and basic circuits, integrated circuit layout and fabrication, dynamic logic, circuit design and layout strategies for large scale CMOS circuits, estimation and optimization of logic speed.
b. Prerequisites: ELEG 3214 or ELEG 3933 and ELEG 2904
c. Technical Elective

Specific Goals for the Course

1. Specific outcomes of instructions
   After completing this course, students should be able to do the following:
   - Design large scale digital integrated circuits
   - Layout large scale digital integrated circuits (except for knowledge of CAD tools)
   - Optimize propagation delay in CMOS digital circuitry on an integrated circuit chip

2. Student outcomes listed in Criterion 3 addressed by the course
   (a) Students are able to apply mathematics in analyzing Integrated Circuits.
   (c) Students are able to design circuits to meet performance specifications.

List of Topics

1. MOSFET Review (1 class)
2. Static CMOS Gates (2 classes)
3. Transmission Gates (1 class)
4. Dynamic Storage (1 class)
5. Multiplexers (1 class)
6. Latches & Registers (2 classes)
7. Overview of Semiconductor Fabrication (2 classes)
8. A Simplified CMOS Process (2 classes)
9. Layout of Static CMOS Gates (2 classes)
10. Simplified CMOS Geometric Design Rules (1 class)
11. Design Partitioning & Layout of Large Circuits (3 classes)
12. MOSFET I/V Characteristics & Parasitic Capacitance (1 class)

13. Non-Ideal MOSFET Characteristics at Small Line Widths (2 classes)
14. Mid Term Exam (1 class)
15. Inverter D.C. Characteristics & Threshold (2 classes)
16. Switch-Level RC Delay Model for Inverters (2 classes)
17. The Shallow Trench Isolation CMOS Process (2 classes)
18. Sheet Resistance & MOSIS Electrical Design Rules (1 class)
19. MOSIS Scalable CMOS Geometrical Design Rules (2 classes)
20. RC Delay Models for Gates & Networks & Logical Effort (5 classes)
21. Minimizing Delay in Gate Networks (4 classes)
22. Adder Design & Layout (3 classes)