ELEG 5253 - INTEGRATED CIRCUIT DESIGN LABORATORY I

Spring Semester, 2007

Catalog Data: 2006-07
ELEG 5253. Integrated Circuit Design Laboratory I. Credit 3. Design and layout of large scale digital integrated circuits. Students design, check and simulate digital integrated circuits which will be fabricated, and tested in I.C. Design Laboratory II. Topics include computer aided design, circuit timing, and wire delay. Prerequisites: ELEG 4233 and 4203.

Textbook:
CMOS VLSI Design: A Circuits and Systems Perspective, by Neil H.E. Weste & David Harris, Third Edition

Reference:
None

Coordinator:
R. L. Brown, Associate Professor of Electrical Engineering

Goals:
The principal goal is to teach students everything necessary to design a large digital integrated circuit, and give them the experience of actually designing one. A secondary goal is to teach them how to manage circuit timing and wire delay.

Prerequisites by Topic:

1. Digital and analog electronics (ELEG 2903 & ELEG 3213 or equivalent)
2. The fundamentals of CMOS digital integrated circuit design (ELEG 4233)

Topics:

1. Design Methodology (1 class)
2. Floor Planning (1 class)
3. IC Layout Using ICStation (5 classes)

4. Schematic Capture Using Design Architect (3 classes)
5. Simulation Using QuickSimII (3 classes)
6. Simulation Using Digital Unidirectional Transistors (1 class)
7. Clock Timing in Registers (4 classes)
8. Specifying Timing Using Technology Files (3 classes)
9. Mentor Graphics Design Viewpoints (1 class)
10. Mentor Graphics Components & Interfaces (3 classes)

11. Properties & Parameters in Mentor Graphics (1 class)
12. Exam (1 class)
13. Clock Driver Design (1 class)
14. MOSIS I/O Pads (1 class)
15. Layout Versus Schematic Comparison Using ICTrace (3 classes)
16. Making Simulated Timing Depend on Load Capacitance (1 class)

17. CIF (Cal Tech Intermediate Form) (2 classes)
18. Latchup (2 classes)
19. Two Phase Clock Generators (0 classes)
20. Wire Delay (6 classes)

Laboratory Project:

Working in teams of three, students design, lay out, check, and simulate integrated circuits of about 5000 transistors. The layouts will be manufactured and shipped back for testing in time to be tested in I.C. Design Lab II.

Computer Usage:

Most of the class is devoted to learning and using Mentor Graphics for chip layout, simulation, and checking. Most of the time spent on the project is spent in front of a SUN workstation.

Computers: SUN workstation

Languages: Mentor Graphics

Operating Systems: UNIX

ABET category content as estimated fy faculty member who prepared this course description:

Engineering Science:	0 credits or 0%.
Engineering Design:	3 credits or 100%.